UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,844	09/28/2006	Akira Ohuchi	Q97404	3674

23373 7590 05/11/2010

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
HARRISTON, WILLIAM A	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
05/11/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

sughrue@sughrue.com
PPROCESSING@SUGHRUE.COM
USPTO@SUGHRUE.COM

Office Action Summary	Application No.	Applicant(s)	
	10/594,844	OHUCHI ET AL.	
	Examiner	Art Unit	
	WILLIAM HARRISTON	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6,8,9 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,4,6,8,9 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/26/2010 have been fully considered but they are not persuasive. Applicant has argued that the prior art does not teach a structure in which a solder resist overlaps an electrode pad in a solder mask defined structure. The Examiner respectfully disagrees. As can be clearly seen in figure 2b of the Qi reference, the solder resist 250 overlaps with the electrode pads 242 at least in a horizontal plane.

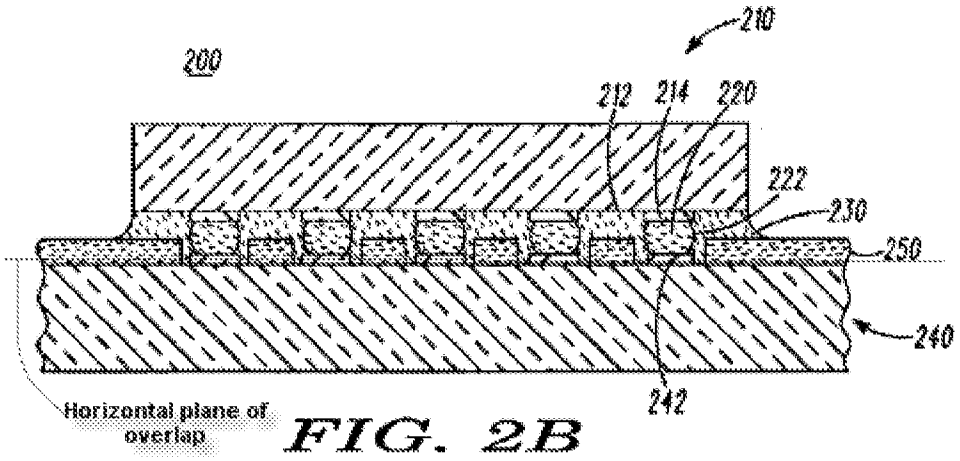

FIG. 2B

The applicant is respectfully advised that claims in a pending application should be given their broadest reasonable interpretation. *In re Pearson*, 181 USPQ 641 (CCPA 1974). See also *In re American Academy of Science Tech Center*, 70 USPQ2d. 1827 (Fed. Cir. May 13, 2004). MPEP § 2111.01. Examiner has interpreted the claimed "overlaps" limitation to mean that the electrode pad and the solder mask share some common property or dimension. In the instant case, they share a common horizontal plane.

Claim Rejections - 35 USC § 103

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 2, 4, 6, 8, 9 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qi US 6774497 taken with Fujimori US 20040046252 A1.

4. Regarding claim 1, Qi disclose a semiconductor device (200 in figure 2b) comprising:

a wiring board (240 in figure 2b) in which electrode pads (242 in figure 2b) are formed on the surface thereof;

a semiconductor element (210 in figure 2b) which is disposed on the wiring board and in which electrodes (214 in figure 2b) are formed on the surface thereof;

bumps (220 in figure 2b) for connecting said electrodes (214 in figure 2b) to said electrode pads (242 in figure 2b);

said bumps (220 in figure 2b) being formed from solder (see column 6 lines 12-14 of Qi); and

an underfill material (230 in figure 2b) filled between said wiring board (240 in figure 2b) and said semiconductor element (210 in figure 2b) to embed said bumps (220 in figure 2b), wherein said wiring board comprises a solder resist (250 in figure 2b)

disposed on the surface of the side on which said electrode pads (242 in figure 2b) are formed;

wherein apertures for exposing said electrode pads (242) are formed on the solder resist (Examiner has interpreted "apertures" to be openings formed in the solder resist layer, this feature is disclosed at column 6, line 49-51) and the thickness of said solder resist in the area excluding the area directly above said electrode pads is equal to or greater than the thickness of said underfill resin disposed on said solder resist in said area between said wiring board a said semiconductor element (see column 7 lines 1-6). Qi further discloses wherein the solder resist 250 in figure 2b) overlaps the electrode pads (242 in figure 2b) in a solder mask defined structure. See Response to Arguments above. Qi further discloses wherein the volume of said bumps (220 in figure 2b) is greater than the volume of said apertures. See Response to Arguments from Office Action dated 10/27/2009.

Qi does not disclose the underfill material is resin.

However, Fujimori does disclose a resin underfill material (173 in figure 43). It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Fujimori with the teachings of Qi because forming an under fill material from resin would reduce heat induced deformation between a semiconductor element and a wiring board, which would improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

5. Regarding claim 2, Qi taken with Fujimori disclose the device of claim 1 for the reasons stated above. Qi further disclose the device wherein the thickness of said underfill resin disposed on said solder resist is 50 micrometers or less. See Qi column 7, lines 1-6. Qi discloses the underfill material may have a thickness of 20% of the connective bump height. The connective bump height of Qi is 4.5 mils, See column 7 lines 17-20. Therefore the underfill material will have a thickness of 0.9 mils. 0.9 mils = 22.9 micrometers..

6. Regarding claim 4, Qi taken with Fujimori disclose the device of claim 3 for the reasons stated above. Qi further disclose the device wherein the thickness of said solder resist (250) is 30 micrometers or more. See Qi column 7, lines 1-6. Qi discloses the solder resist (250 in figure 2b) may have a thickness of 80% of the connective bump height. The connective bump height of Qi is 4.5 mils, See column 7 lines 17-20. Therefore the solder resist will have a thickness of 3.6 mils. 3.6 mils = 91.5 micrometers..

7. Regarding claim 6, Qi discloses a method for manufacturing a semiconductor device, said method comprising the steps of:

forming bumps (120 in figure 1) on at least said electrode pads (114 in figure 1);

depositing an underfill material (130 in figure 1) on at least a portion of the area in which said semiconductor element (110 in figure 1) is to be mounted on said wiring board (240 in figure 2a);

pressing said semiconductor element to said wiring board to connect said electrode pads, said bumps, and said electrodes to each other; (see column 7 lines 41-

46)

melting and then solidifying said bumps to join said electrodes to said electrode pads by way of said bumps; see column 7 lines 41-46) and

curing said resin material and forming an underfill resin so that said bumps become embedded between said wiring board and said semiconductor element; (see column 8 lines 4-8)

wherein the distance between said wiring board and said semiconductor element is controlled during the melting of said bumps in said joining step; (see column 8 lines 30-33)

and the thickness of said solder resist in the area excluding the area directly above said electrode pads is equal to or greater than the thickness of said underfill material disposed on said solder resist in said area between said wiring board and said semiconductor element after said underfill material has been formed. (see column 7 lines 1-6). Qi further discloses wherein the solder resist (250 in figure 2b) overlaps the electrode pads (242 in figure 2b) in a solder mask defined structure. See Response to Arguments above. Qi further discloses wherein the volume of said bumps (220 in figure 2b) is less than the volume of said apertures in the step of forming said bumps. See Response to Arguments from Office Action dated 10/27/2009.

Qi does not disclose the underfill material is resin.

However, Fujimori does disclose a resin underfill material (173 in figure 43). It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Fujimori with the teachings of Qi because forming an

under fill material from resin would reduce heat induced deformation between a semiconductor element and a wiring board, which would improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

8. Regarding claim 8, Qi taken with Fujimori disclose the method of claim 6 for the reasons stated above. Qi further discloses the method wherein the thickness of said underfill resin disposed on said solder resist is 50 micrometers or less. See Qi column 7, lines 1-6. Qi discloses the underfill material may have a thickness of 20% of the connective bump height. The connective bump height of Qi is 4.5 mils, See column 7 lines 17-20. Therefore the underfill material will have a thickness of 0.9 mils. 0.9 mils = 22.9 micrometers..

9. Regarding claim 9, Qi taken with Fujimori disclose the method of claim 6 for the reasons stated above. Qi further discloses the method wherein the distance between said wiring board and semiconductor element is controlled by controlling the relative position of said semiconductor element with respect to said wiring board in said joining step. See column 7.

10. Regarding claim 11, Qi taken with Fujimori disclose the method of claim 6 for the reasons stated above. Qi further discloses an underfill material to which a chemical capable of removing an oxide film is added is used as an underfill material. See column 7, line 52- column 8.

Qi does not disclose the underfill material is resin. However, Fujimori does

disclose a resin underfill material (173 in figure 43 of Fujimori). It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Qi with the teachings of Fujimori because forming an under fill material from resin would reduce heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

11. Regarding claim 12, Qi taken with Fujimori disclose the device of claim 6 for the reasons stated above. Qi taken with Fujimori no dot disclose the step of carrying out a plasma treatment. However, plasma treatment is well known in the art for growing largely crystalline oxide coating, which present high hardness and a continuous barrier, on metals. One of ordinary skill in the art would be motivated to perform a plasma treatment for the purpose of offering protection against wear, corrosion, and heat.

12. Regarding claims 13 and 15, Qi taken with Fujimori disclose the device of claim 1 and the method of claim 6 for the reasons stated above. Qi further discloses wherein the thickness of the solder resist (250 in figure 2b) is about 30 micrometers. See Qi column 7, lines 1-6. Qi discloses the solder resist (250 in figure 2b) may have a thickness of 40% of the connective bump height. The connective bump height of Qi is 4.5 mils, See column 7 lines 17-20. Therefore the solder resist will have a thickness of 1.8 mils. 3.6 mils = 45.7 micrometers. The claim does not preclude a solder resist having a thickness of 45.7 micrometers

13. Regarding claims 14 and 16, Qi taken with Fujimori disclose the device of claim 1 and the method of claim 6 for the reasons stated above. Qi further discloses wherein:

the thickness of the solder resist (250 in figure 2b) in the area excluding the area directly above the electrode pads is at least four times greater than the thickness of the underfill resin (230 in figure 2b) disposed on the solder resist in the area between the wiring board 240 and the semiconductor element 210. Qi column 7 lines 1-6 disclose the underfill material (230 in figure 2b) may have a thickness equal to 20% of the connective bump height. Qi further discloses the solder resist (250 in figure 2b) may have a thickness equal to 80% of the connective bump height.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM HARRISTON whose telephone number is (571)270-3897. The examiner can normally be reached on Monday - Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. H./
Examiner, Art Unit 2826
5/3/2010

/Leonardo Andújar/
Primary Examiner, Art Unit 2826